

U.S.S.N. 10/677,158

Specification Amendments

Please replace paragraph 0018 with the following re-written paragraph:

"Referring to Figure 1 is shown a cross sectional schematic of an exemplary CMOS transistor having gate structure including a high-k dielectric gate stack region according to an embodiment of the present invention. Shown is semiconductor substrate 12, for example a silicon substrate including lightly doped regions e.g., 14A, source/drain regions, e.g., 14B and shallow trench isolation regions, e.g., 16 formed in the silicon substrate by conventional methods known in the art. The regions 14A and 14B are typically formed following the formation of the gate structure. The gate dielectric portion of the gate structure is formed of multiple layers including for example, an interfacial silicon dioxide layer 18A, and high-K dielectric portion 18B. A polysilicon gate electrode portion 18C is formed over the gate dielectric portion. The gate structure is formed by conventional methods including photolithographic patterning and anisotropic etching steps following blanket deposition of the various layers including an uppermost polysilicon layer.

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Please replace paragraph 0032 with the following re-written paragraph:

For example, referring to Figure 3A, is shown a graph of exemplary data (CV curve) with capacitance on the vertical axis and applied gate Voltage on the horizontal axis in an exemplary NMOS devices. Lines A, B, and C respectively represent 'as deposited' (A), i.e., with no plasma treatment of the gate stack including a high-K dielectric, followed by shown juxtaposed to devices formed having the gate stack exposed to increased times of a plasma treatment in hydrogen e.g., 30 min (B), and 60 min (C). Line D, by contrast, represents a device formed with the gate stack exposed to a plasma treatment followed by an annealing treatment in nitrogen (N<sub>2</sub>) according to preferred embodiments, showing demonstrating a significant improvement in the CV curve characteristics including flatband Voltage derived therefrom by known methods.

Please replace paragraph 0033 with the following re-written paragraph:

Referring to Figure 3B, is shown a graph of exemplary data of CMOS devices with the flatband Voltage on the vertical axis

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and the gate stack treatment condition separated on the horizontal axis. Gate stack treatment condition A1 corresponds to 'as deposited' condition (without a plasma treatment or anneal treatment of the gate stack); gate stack treatment conditions B1, C1, and D1, respectively correspond to a 10, 30, and 60 minute H<sub>2</sub> plasma treatment according to preferred embodiments. Gate stack treatment condition E1, by contrast, shows a 60 minute H<sub>2</sub> plasma treatment followed by an annealing treatment according to preferred embodiments, showing a significant improvement in flatband Voltage.

Please replace paragraph 0035 with the following re-written paragraph:

Referring to Figure 4 is a process flow diagram including several embodiments of the present invention. In a first process 401, an interfacial oxide layer is provided over a silicon substrate. In process 403, at least one high-K dielectric layer, preferably HfO<sub>2</sub>, is deposited over the interfacial oxide. In process 405, a polysilicon layer is deposited. In process 407, the polysilicon layer is patterned and etched through a thickness portion of the polysilicon and high-K dielectric to form a gate

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structure. In process 409, a plasma treatment is carried out according to preferred embodiments. In process 411, a post plasma treatment anneal is carried out according to preferred embodiments. In process 413, conventional processes are carried out to complete the CMOS device.

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